

## TD541S-4xH(L)x DFN package integrated isolated DC-DC converter

### Features

- Ultra-small, ultra-thin, chip scale DNFpackage
- Baud rate up to 150Mbps
- Low communication delay
- Integrate 5V efficiently power supply
- High isolation to 5000VDC
- High HBM:  $\pm 8\text{kV}$
- High CMTI:  $75\text{ kV}/\mu\text{s}$ (typical)
- Industrial operating ambient temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### Applications

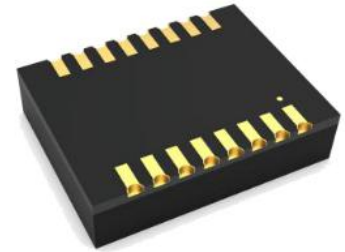
- Industrial automation systems
- Motor control
- Medical equipment
- Test and measurement
- Isolated ADC, DAC

### Functional Description

TD541S-4xH(L)x is a family of high-performance reinforced digital isolators with an integrated isolated DC-DC converter. TD541S-4xH(L)x eliminate the need for a separate, isolated power supply, which results in a small form factor, total isolation solution. The power supply voltage of TD541S-4xH(L)5 is 5V and its isolated power is 5V. The power supply voltage of TD541S-4xH(L)3 is 5V and its isolated power is 3.3V.

TD541S-40H(L)x device has four forward and one reverse-direction channels. TD541S-41H(L)x device has three forward and one reverse-direction channels. TD541S-42H(L)x device has two forward and two reverse-direction channels. TD541S-43H(L)x device has one forward and three reverse-direction channels. TD541S-44H(L)x device has four reverse-direction channels. And has fail-safe mode options if the input signal is lost the chip with suffix L defaults to output low level and the chip with suffix H defaults to output high level.

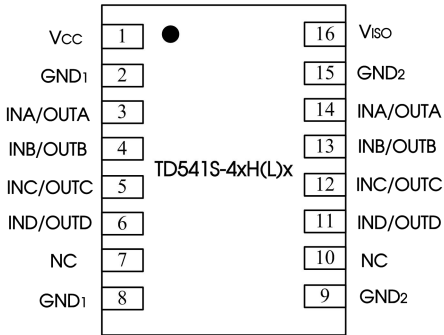
### Package



# Contents

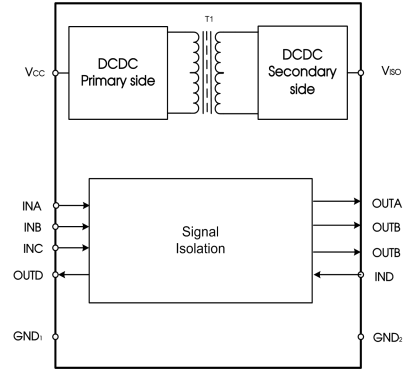
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## Pin Connection



Note: All GND<sub>1</sub> pins are internally connected;  
All GND<sub>2</sub> pins are internally connected.

## Internal Block Diagram



Take TD541S-41H(L)x as an example here.

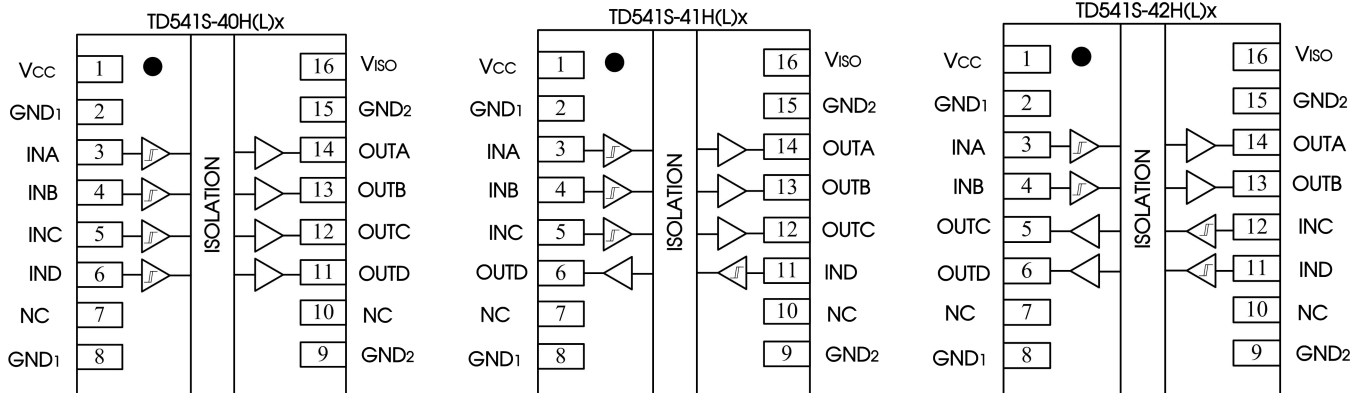
## Function Table

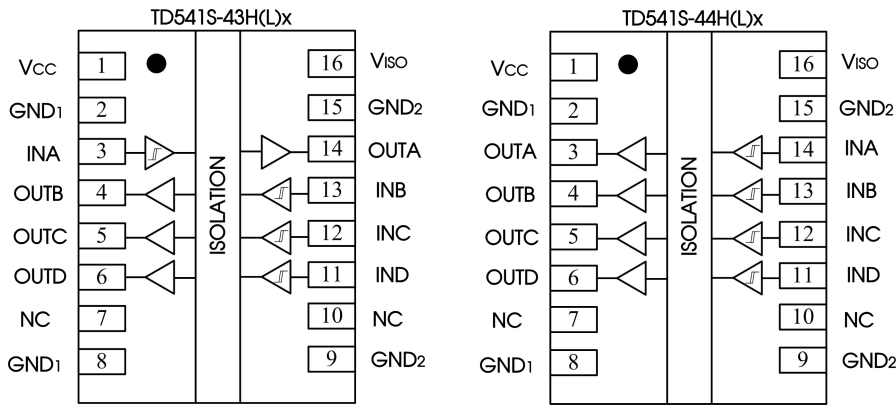
Table 2. Operation Mode Table

V <sub>CC</sub>	Input	Output	Operation
PU	H	H	Normal operation mode: A channel's output follows the input state
	L	L	
	OPEN	Default	Default output fail-safe mode: If a channel's input is left open, its output goes to the default high level. (In the default condition, the output is high for TD541S-4xHx and low for TD541S-4xLx)
PD	X	Undetermined	

Note:  
1. PU = Powered up (V<sub>CC</sub> ≥ 3.1 V); PD = Powered down (V<sub>CC</sub> ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.  
2. The outputs are in undetermined state when V<sub>CC</sub> < 2.1V.

## Pin Descriptions





Pin Number	Pin Name	Pin Functions
1	V <sub>CC</sub>	Power supply(Side 1).
2	GND <sub>1</sub>	Ground(Side 1)
3	INA/OUTA	Digital input/output(Side 1)
4	INB/OUTB	Digital input/output(Side 1)
5	INC/OUTC	Digital input/output(Side 1)
6	IND/OUTD	Digital input/output(Side 1)
7	NC	No Connect
8	GND <sub>1</sub>	Ground(Side 1)
9	GND <sub>2</sub>	Ground(Side 2)
10	NC	No Connect
11	IND/OUTD	Digital input/output(Side 2)
12	INC/OUTC	Digital input/output(Side 2)
13	INB/OUTB	Digital input/output(Side 2)
14	INA/OUTA	Digital input/output(Side 2)
15	GND <sub>2</sub>	Ground(Side 2)
16	V <sub>ISO</sub>	Insulation power output .

## Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

PARAMETERS	UNIT
Supply voltage	-0.5V to +6V
Input voltage	-0.5V to V <sub>CC</sub> +0.5V
Output current	-20mA to +20mA ( TD541S-4xH(L)5 )
	-15mA to +15mA ( TD541S-4xH(L)3 )
Receiver Output current	< 150°C
Operating temperature range	-40°C to +125°C
Storage temperature range	-65°C to +150°C

Important: Exposure to absolute maximum rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the "Absolute Maximum Ratings" may result in permanent damage. All voltage values are referenced to the reference ground (GND).Maximum voltage shall to not exceed 6V.

## Recommended Operating Conditions

PARAMETERS		Min.	Nom.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	High-level Input Voltage	2			V
V <sub>IL</sub>	Low-level Input Voltage			0.8	V
I <sub>OH</sub>	High-level Output Current	-4			mA
I <sub>OL</sub>	Low-level Output Current			4	mA

T <sub>A</sub>	Ambient Temperature		-40	125	°C
P <sub>D</sub>	Maximum Power Dissipation	V <sub>CC</sub> = 5.25V, I <sub>LOAD</sub> =130mA, all digital channels input :f=100MHz ; Duty=50%		1.02	W
DR	Data Rate		0	150	Mbps

General test conditions and V<sub>CC</sub>= 5V, T<sub>A</sub> = 25°C (unless otherwise specified).

Note: V<sub>CCI</sub> = input side supply; V<sub>CCO</sub> = output side supply.

## Electrical Characteristics

TD541S-4xH(L)5: 5 V Input, 5 V output : V<sub>CC</sub>= 5 V ± 5%, T<sub>A</sub> = -40 to 125°C.

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
V <sub>ISO</sub>	Isolated supply voltage	External I <sub>ISO</sub> =0 to 50mA	4.65	5.10	5.60	V
		External I <sub>ISO</sub> =0 to 130mA	4.5	5.10	5.60	
V <sub>ISO(LINE)</sub>	DC line regulation	I <sub>ISO</sub> =50mA, V <sub>CC</sub> =4.75V to 5.25V			1.2%	
V <sub>ISO(LOAD)</sub>	DC load regulation	I <sub>ISO</sub> =0 to 130mA		8%	15%	
V <sub>CC(UVLO+)</sub>	V <sub>CC</sub> under voltage threshold when supply voltage is rising		2.79	3.1	3.41	V
V <sub>CC(UVLO-)</sub>	V <sub>CC</sub> under voltage threshold when supply voltage is falling		1.89	2.1	2.31	V
V <sub>IT+(IN)</sub>	Positive-going input threshold				2.0	V
V <sub>IT-(IN)</sub>	Negative-going input threshold		0.8			V
V <sub>I(HYS)</sub>	Input threshold hysteresis		0.30	0.44	0.50	V
I <sub>IH</sub>	High-level input leakage current	V <sub>IH</sub> =V <sub>CCI</sub> at INx			20	uA
I <sub>IL</sub>	Low-level input leakage current	V <sub>IH</sub> =0V at INx	-20			uA
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA, Figure 8	V <sub>CCO</sub> - 0.4	V <sub>CCO</sub> - 0.2		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA, Figure 8		0.2	0.4	V
CMTI	Common-mode transient immunity	V <sub>I</sub> = 0 V or V <sub>CC</sub>	75	100		kV/us
V <sub>ISO(RIP)</sub>	Output ripple on isolated supply (pk-pk)	20MHz bandwidth, C <sub>LOAD</sub> =0.1uF    20uF, I <sub>ISO</sub> =130mA		30	75	mV
V <sub>I-O</sub>	Isolation voltage	Leakage current <1mA.			5000	VDC
	Insulation resistance	At 500VDC			1000	MΩ
ESD	HBM	All pins			±8	kV
	Contact	Power pins			±4	kV

TD541S-4xH(L)3: 5 V Input, 3.3 V output : V<sub>CC</sub>= 5 V ± 5%, T<sub>A</sub> = -40 to 125°C.

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
V <sub>ISO</sub>	Isolated supply voltage	External I <sub>ISO</sub> =0 to 50mA	3.1	3.4	3.72	V
		External I <sub>ISO</sub> =0 to 130mA	3	3.4	3.72	
V <sub>ISO(LINE)</sub>	DC line regulation	I <sub>ISO</sub> =50mA, V <sub>CC</sub> =4.75V to 5.25V			1.2%	
V <sub>ISO(LOAD)</sub>	DC load regulation	I <sub>ISO</sub> =0 to 130mA		8%	15%	
V <sub>CC(UVLO+)</sub>	V <sub>CC</sub> under voltage threshold when supply voltage is rising		2.79	3.1	3.41	V
V <sub>CC(UVLO-)</sub>	V <sub>CC</sub> under voltage threshold when supply voltage is falling		1.89	2.1	2.31	V
V <sub>IT+(IN)</sub>	Positive-going input threshold				2.0	V
V <sub>IT-(IN)</sub>	Negative-going input threshold		0.8			V
V <sub>I(HYS)</sub>	Input threshold hysteresis		0.30	0.44	0.50	V
I <sub>IH</sub>	High-level input leakage current	V <sub>IH</sub> =V <sub>CCI</sub> at INx			20	uA
I <sub>IL</sub>	Low-level input leakage current	V <sub>IH</sub> =0V at INx	-20			uA
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA, Figure 8	V <sub>CCO</sub> - 0.4	V <sub>CCO</sub> - 0.2		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA, Figure 8		0.2	0.4	V
CMTI	Common-mode transient immunity	V <sub>I</sub> = 0 V or V <sub>CC</sub> ;	75	100		kV/us
V <sub>ISO(RIP)</sub>	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C <sub>LOAD</sub> =0.1uF    20uF, I <sub>ISO</sub> =130mA		30	75	mV
V <sub>I-O</sub>	Isolation voltage				5000	VDC
	Insulation resistance				1000	MΩ

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
ESD $V_{ISO(RIP)}$	HBM	All pins			±8	kV
	Contact	Power pins			±4	kV

### Supply Current Characteristics

General test conditions and  $V_{CC}=5V$ ,  $T_a=25^\circ C$  (unless otherwise specified).

TD541S-4xH(L)5: 5 V Input, 5 V output :  $V_{CC}=5V \pm 5\%$ ,  $T_A=-40$  to  $125^\circ C$ .

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
$I_{DD}$	Static current from supply	$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , H5: $V_i=L$ L5: $V_i=H$		15	25	mA
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , H5: $V_i=H$ L5: $V_i=L$		12	23	
	Maximum Operating Current	$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=1Mbps$ ; Duty=50% ;		17	30	
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=10Mbps$ ; Duty=50% ;		34	60	
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=100Mbps$ ; Duty=50% ;		43	70	
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=150Mbps$ ; Duty=50% ;		46	80	

TD541S-4xH(L)3: 5 V Input, 3.3 V output :  $V_{CC}=5V \pm 5\%$ ,  $T_A=-40$  to  $125^\circ C$ .

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
$I_{DD}$	Static current from supply	$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , H3: $V_i=L$ L3: $V_i=H$		11	22	mA
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , H3: $V_i=H$ L3: $V_i=L$		9	20	
	Maximum Operating Current	$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=1Mbps$ ; Duty=50% ;		13	35	
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=10Mbps$ ; Duty=50% ;		15	50	
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=100Mbps$ ; Duty=50% ;		30	60	
		$V_{CC}=5V \pm 5\%$ ; $I_{ISO}=0$ , All channels switching : $f=150Mbps$ ; Duty=50% ;		40	80	

Note:

- $V_{CCI}$  = input side supply ;  $V_{CCO}$  = output side supply.
- When  $T_A > 105^\circ C$ , Current available to isolated supply should be reduced by  $2mA/^\circ C$ .

### Transmission Characteristics

General test conditions and  $V_{CC}=5V$ ,  $T_a=25^\circ C$  (unless otherwise specified).

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
DR	Data Rate		0		150	Mbps
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Time	Figure 8		8.0	13.0	ns
PWD	Pulse Width Distortion   $t_{PLH} - t_{PHL}$			0.2	4.5	ns
$t_{rk(O)}$	Channel-to-channel Output Skew Time			0.4	2.5	ns
$t_{rk(PP)}$	Part-to-part Skew Time			2.0	4.5	ns
$t_r$	Output Signal Rise Time	Figure 8		2.5	4.5	ns

PARAMETERS		CONDITIONS	Min.	Nom.	Max.	Unit
$t_f$	Output Signal Fall Time			2.5	4.5	ns

Note:

1.  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected and the outputs switching in the same direction while driving identical loads.
2.  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## Physical Specifications

PARAMETERS	Value	Unit
Weight	0.9(Typ.)	g

## Test Circuits

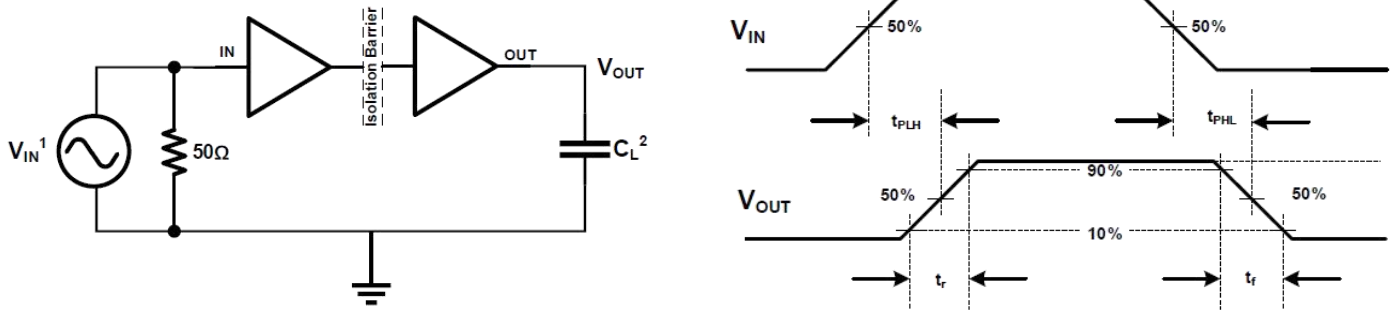


Figure 8. Timing Characteristics Test Circuit and Voltage Wave forms

Note:

1. A square wave generator generate the  $V_{IN}$  input signal with the following constraints: waveform frequency  $\leq 100\text{kHz}$ , 50% duty cycle,  $t_r \leq 3\text{ns}$ ,  $t_f \leq 3\text{ns}$ . Since the waveform generator has an output impedance of  $Z_{out} = 50\Omega$ , the  $50\Omega$  resistor in the figure is used for matching. There is no need in the actual application.
2.  $C_L$  is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

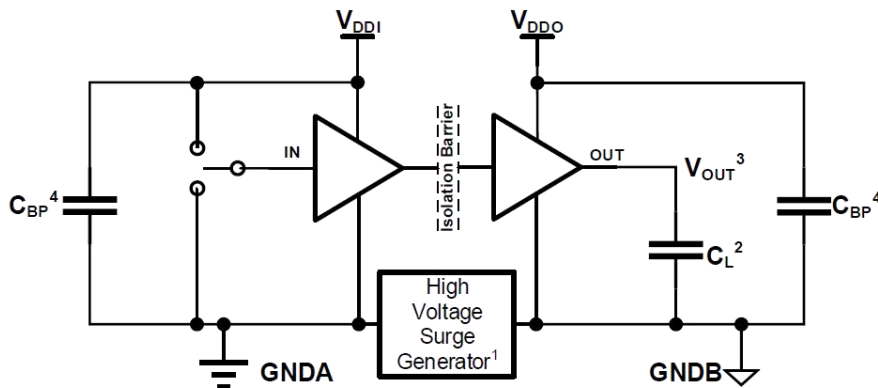


Figure 9. CMTI Test Circuit

Note:

1. The High Voltage Surge Generator generates repetitive high voltage surges with  $> 1.5\text{kV}$  amplitude and  $< 10\text{ns}$  rise time and fall time to reach common-mode transient noise with  $> 150\text{kV}/\mu\text{s}$  slew rate.
2.  $C_L$  is the load capacitance about 15pF together with the instrumentation capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges come.
4.  $C_{BP}$  is the 0.1 to 1uF bypass capacitance.

## Detailed Description

TD541S-4xH(L)x has a high-efficiency, low-emissions isolated dc-dc converter, with high-speed isolated data channels.

The high-speed isolated data channels use a simple ON-OFF keying (OOK) modulation scheme to transmit signal across the SiO<sub>2</sub> isolation capacitors that provide a robust insulation between two different voltage domain and act as a high frequency signal path between the input and the output. The transmitter (TX) modulates the input signal onto the carrier frequency, that is, TX delivers high frequency signal across the isolation barrier in one input state and delivers no signal across the barrier in the other input state. Then the receiver rebuilds the input signal according to the detected

in-band energy. The capacitor-based signal path is fully differential to maximize noise immunity, which is also known as common-mode transient immunity. The capacitively-coupled architecture provides much higher electromagnetic immunity compared to the inductively coupled one.

## Application circuit

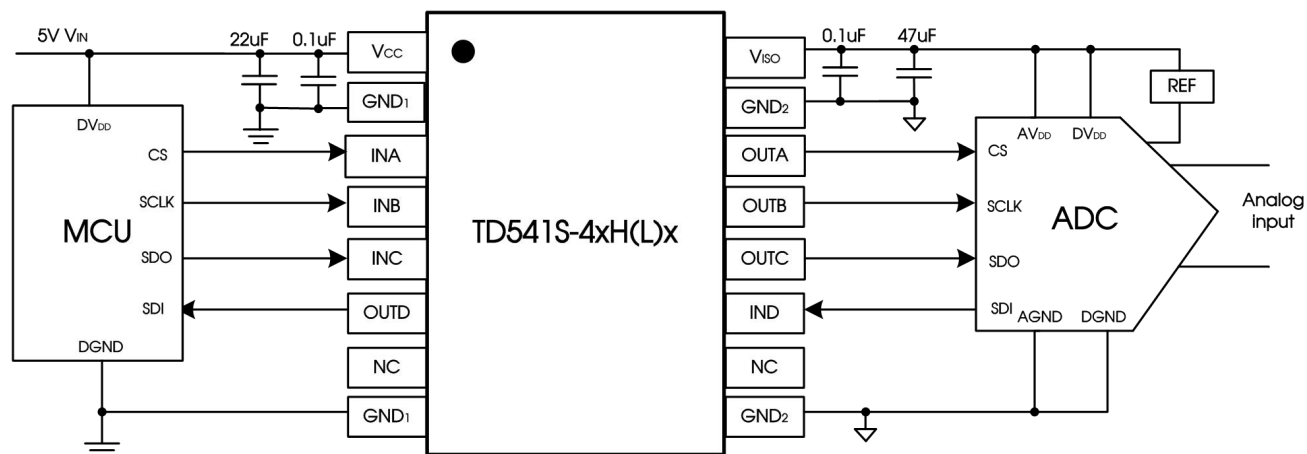
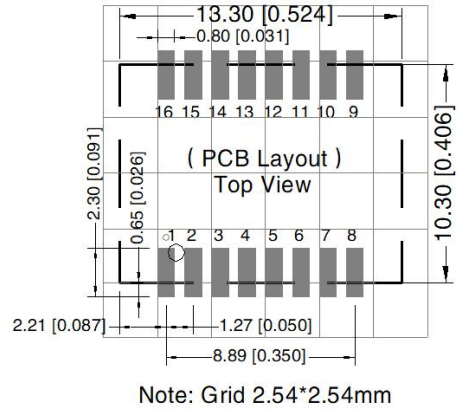
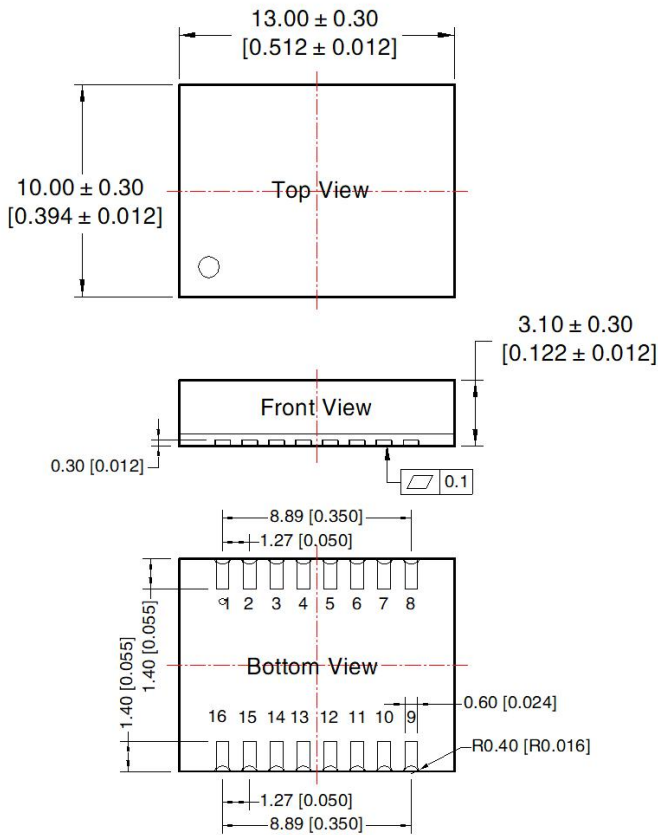


Figure14. Isolated Power and SPI for ADC Sensing Application with TD541S-4xH(L)x

Note: Only model TD541S-4x(L)x is used as an example

## Ordering Information

Part number	Package	Number of pins	Isolated supply voltage	Default output level	Product marking	Tape & Reel
TD541S-40H5	DFN	16	5V	H	TD541S-40H5	300/REEL
TD541S-40L5	DFN	16	5V	L	TD541S-40L5	300/REEL
TD541S-41H5	DFN	16	5V	H	TD541S-41H5	300/REEL
TD541S-41L5	DFN	16	5V	L	TD541S-41L5	300/REEL
TD541S-42H5	DFN	16	5V	H	TD541S-42H5	300/REEL
TD541S-42L5	DFN	16	5V	L	TD541S-42L5	300/REEL
TD541S-43H5	DFN	16	5V	H	TD541S-43H5	300/REEL
TD541S-43L5	DFN	16	5V	L	TD541S-43L5	300/REEL
TD541S-44H5	DFN	16	5V	H	TD541S-44H5	300/REEL
TD541S-44L5	DFN	16	5V	L	TD541S-44L5	300/REEL
TD541S-40H3	DFN	16	3.3V	H	TD541S-40H3	300/REEL
TD541S-40L3	DFN	16	3.3V	L	TD541S-40L3	300/REEL
TD541S-41H3	DFN	16	3.3V	H	TD541S-41H3	300/REEL
TD541S-41L3	DFN	16	3.3V	L	TD541S-41L3	300/REEL
TD541S-42H3	DFN	16	3.3V	H	TD541S-42H3	300/REEL
TD541S-42L3	DFN	16	3.3V	L	TD541S-42L3	300/REEL
TD541S-43H3	DFN	16	3.3V	H	TD541S-43H3	300/REEL
TD541S-43L3	DFN	16	3.3V	L	TD541S-43L3	300/REEL
TD541S-44H3	DFN	16	3.3V	H	TD541S-44H3	300/REEL
TD541S-44L3	DFN	16	3.3V	L	TD541S-44L3	300/REEL

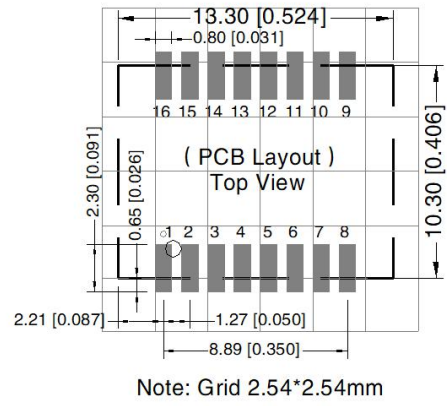
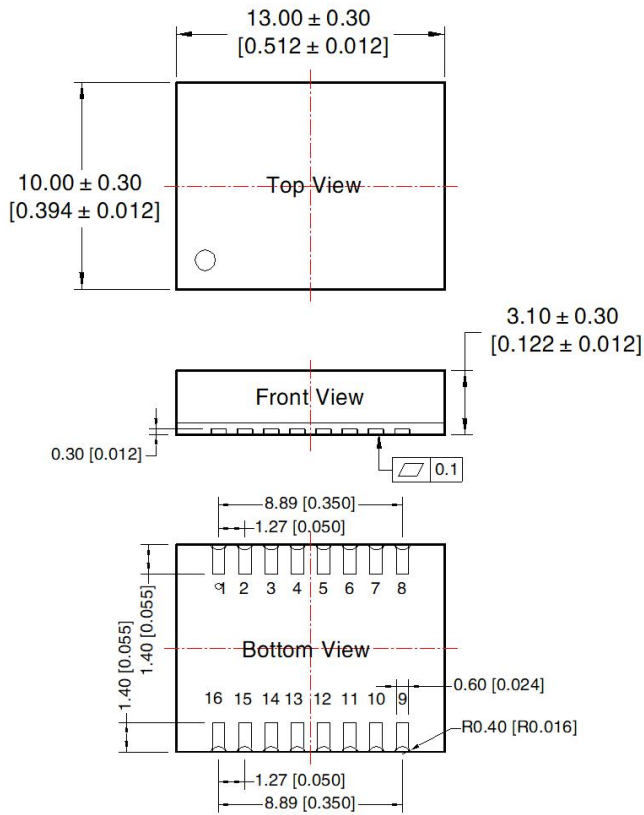


Pin-Out			
Pin	Mark	Pin	Mark
1	V <sub>CC</sub>	9	GND <sub>2</sub>
2	GND <sub>1</sub>	10	NC
3	INA	11	OUTD
4	INB	12	OUTC
5	INC	13	OUTB
6	IND	14	OUTA
7	NC	15	GND <sub>2</sub>
8	GND <sub>1</sub>	16	V <sub>ISO</sub>

Note:  
 Unit: mm[inch]  
 General tolerances:  $\pm 0.10$  [± 0.004]

TD541S-40H(L)x

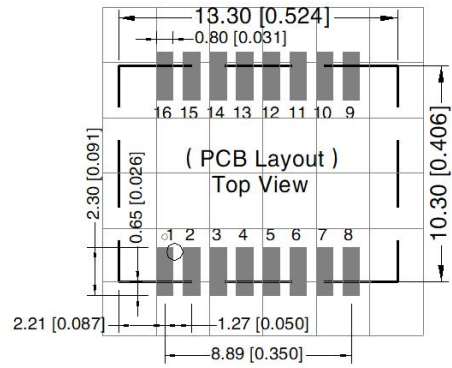
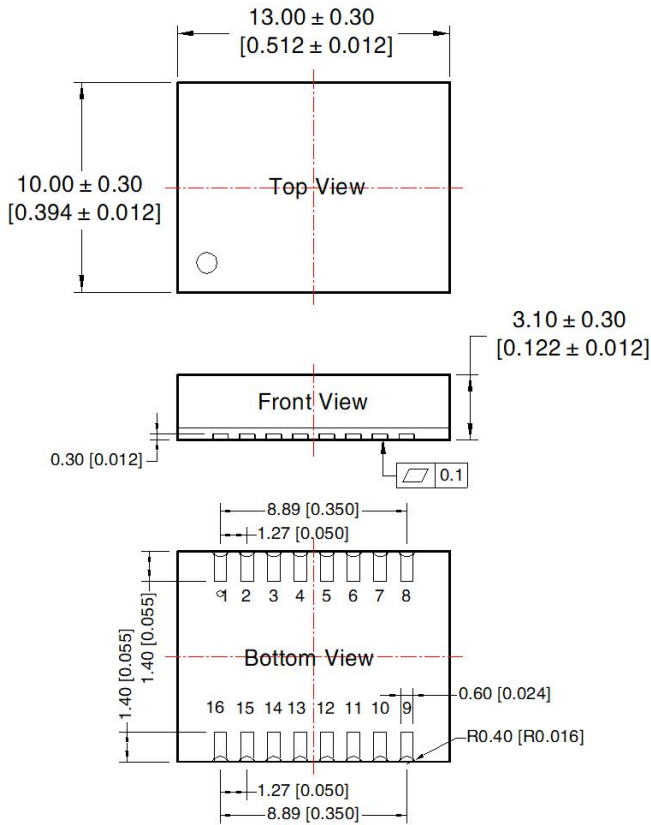




Pin-Out			
Pin	Mark	Pin	Mark
1	V <sub>CC</sub>	9	GND <sub>2</sub>
2	GND <sub>1</sub>	10	NC
3	INA	11	IND
4	INB	12	OUTC
5	INC	13	OUTB
6	OUTD	14	OUTA
7	NC	15	GND <sub>2</sub>
8	GND <sub>1</sub>	16	V <sub>ISO</sub>

Note:  
 Unit: mm[inch]  
 General tolerances:  $\pm 0.10$  [± 0.004]

TD541S-41H(L)x

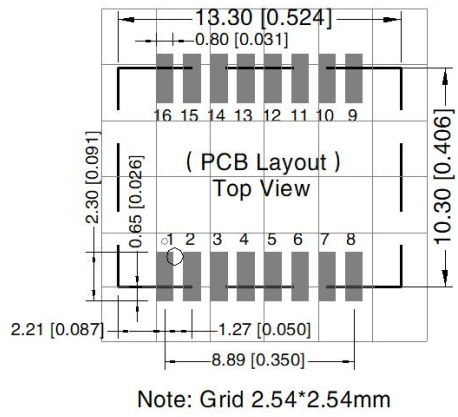
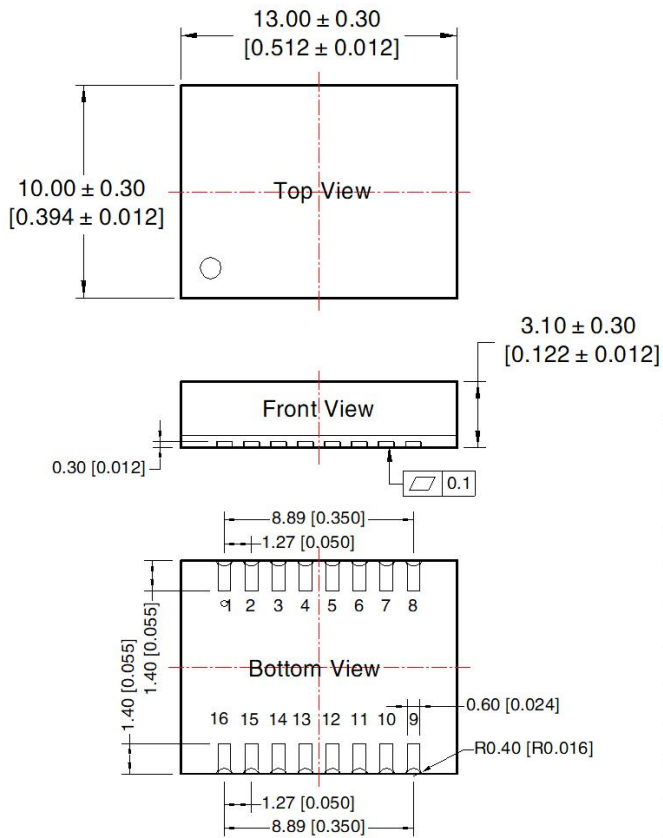


Note: Grid 2.54\*2.54mm

Pin-Out			
Pin	Mark	Pin	Mark
1	V <sub>CC</sub>	9	GND <sub>2</sub>
2	GND <sub>1</sub>	10	NC
3	INA	11	IND
4	INB	12	INC
5	OUTC	13	OUTB
6	OUTD	14	OUTA
7	NC	15	GND <sub>2</sub>
8	GND <sub>1</sub>	16	V <sub>ISO</sub>

Note:  
 Unit: mm[inch]  
 General tolerances:  $\pm 0.10$  [± 0.004]

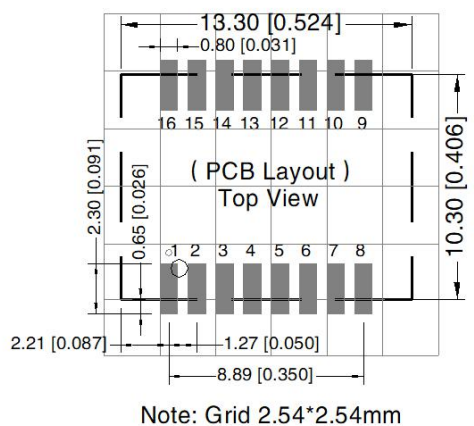
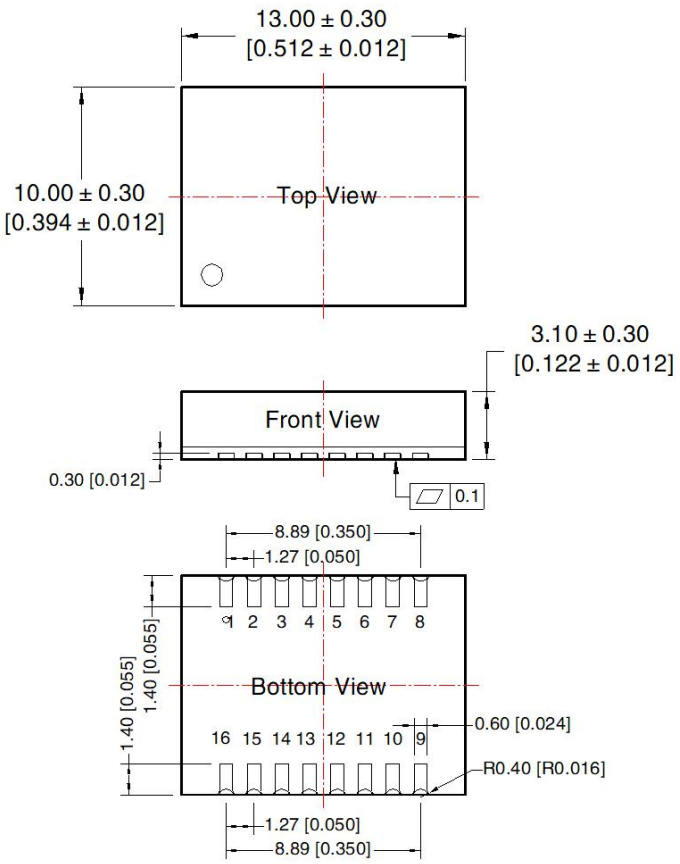
TD541S-42H(L)x



Pin-Out			
Pin	Mark	Pin	Mark
1	V <sub>CC</sub>	9	GND <sub>2</sub>
2	GND <sub>1</sub>	10	NC
3	INA	11	IND
4	OUTB	12	INC
5	OUTC	13	INB
6	OUTD	14	OUTA
7	NC	15	GND <sub>2</sub>
8	GND <sub>1</sub>	16	V <sub>ISO</sub>

Note:  
 Unit: mm[inch]  
 General tolerances:  $\pm 0.10$  [± 0.004]

TD541S-43H(L)x

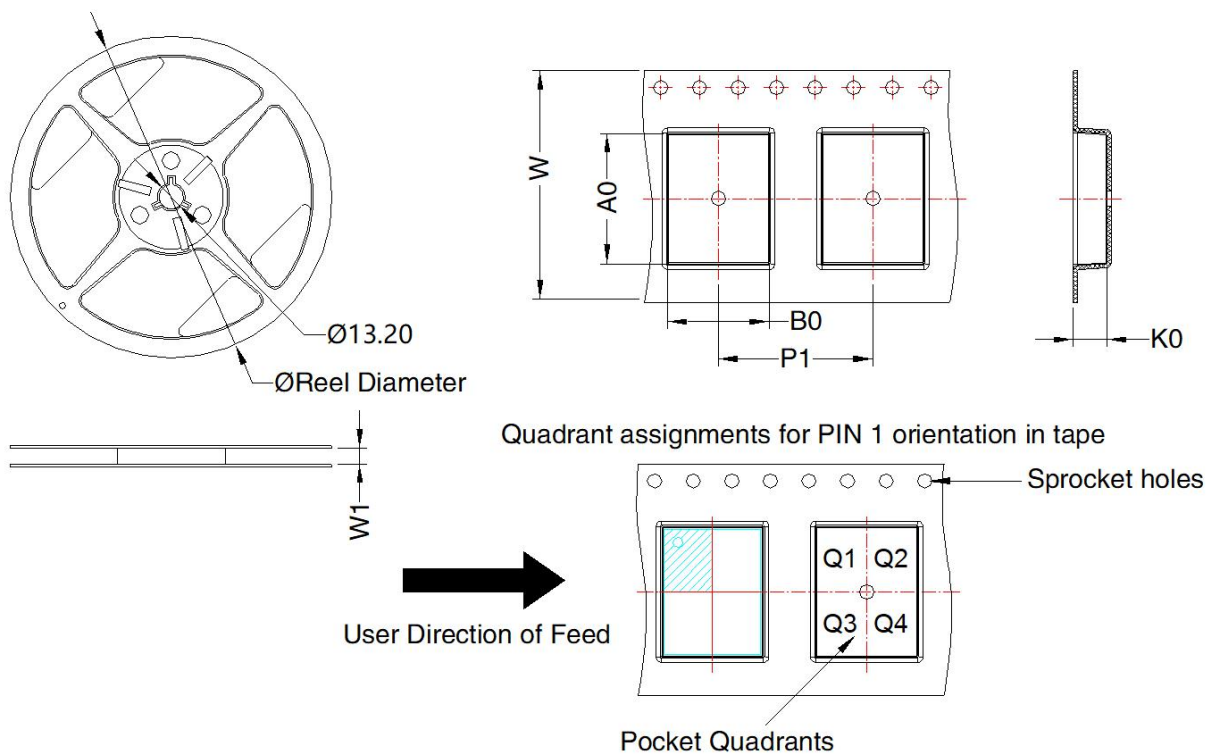


Note: Grid 2.54\*2.54mm

Pin-Out			
Pin	Mark	Pin	Mark
1	V <sub>CC</sub>	9	GND <sub>2</sub>
2	GND <sub>1</sub>	10	NC
3	OUTA	11	IND
4	OUTB	12	INC
5	OUTC	13	INB
6	OUTD	14	INA
7	NC	15	GND <sub>2</sub>
8	GND <sub>1</sub>	16	V <sub>ISO</sub>

Note:  
 Unit: mm[inch]  
 General tolerances:  $\pm 0.10$  [± 0.004]

TD541S-44H(L)x



Device	Package Type	Pin	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TD541S-4xH(L)x	DFN 10x13	20	300	180.0	24.4	13.52	10.52	3.5	16.0	24.0	Q1

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